

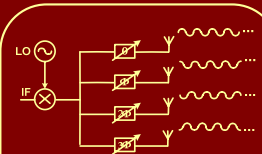
A 0.13 μm CMOS 4-Channel UWB Timed Array Transmitter Chipset with sub-200ps Switches and All-Digital Timing Circuitry

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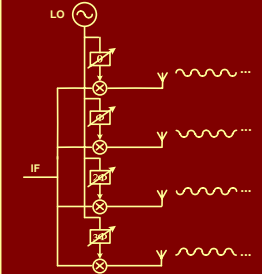
Motivation

- UWB signals allow higher *data rate* for communication systems and higher *depth resolution* for imaging systems;
- UWB multi-antenna transmitters allow focusing signal energy at the desired directions;
- Pulsed-sinusoid waveforms allow for
 - independent control of center frequency and pulse-width (bandwidth);
 - simple generation for antenna arrays.

Narrowband Phased Array Transmitter

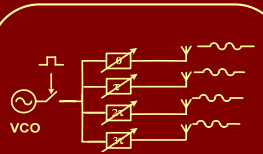


RF Phase-Shifting

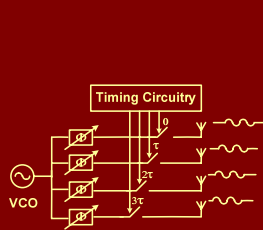


LO Phase-Shifting

UWB (Pulsed-Sinusoid) Timed Array Transmitter



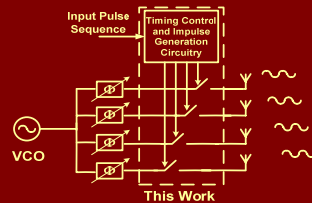
RF True Time Delay (TTD)



Pulse Time-Delaying

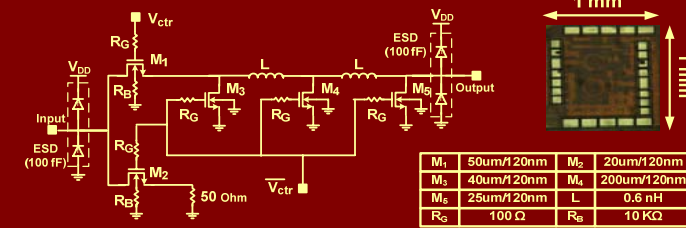
Transmitter Architecture	Advantages	Disadvantages
RF True Time Delay (TTD)	General for all waveforms	On-chip TTD blocks capable of generating nanosecond delay are lossy, have limited bandwidth and consume large footprint
Pulse Time-Delaying	<ul style="list-style-type: none"> - The relative delays of the UWB waveforms can be controlled during pulse generation without using TTD blocks - Digital control of relative delays allows for small delay resolution and large maximum delay in a small area 	Needs phase shifters to align the initial phase of the pulsed sinusoid for coherent signal addition at the target

Transmitter Architecture



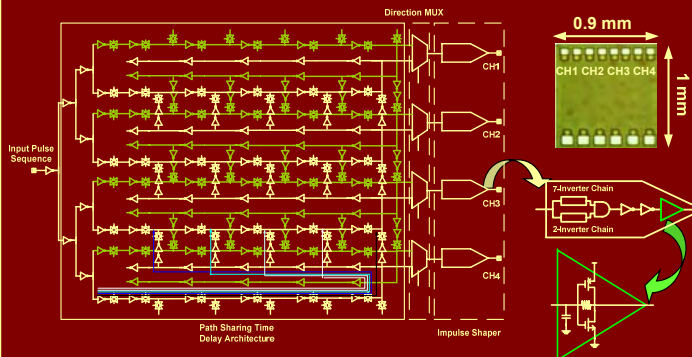
- Chipset includes timing circuitry and UWB pulse-forming switches;
- Fabricated in 0.13 μm CMOS;
- VCO and phase shifters are off-chip.

UWB Pulse-Forming Switch



- Pulse-forming switch is absorptive;
- There are trade-offs in sizing of series and shunt transistors:
 - Larger M_1 reduces low-frequency loss, but, increases high-frequency loss;
 - Larger shunt transistors improve isolation, but, increase loss;
- Rise and fall times are limited by poles of ladder LC network and the resistance at the transistor gate;
- ESD protection circuits are used at the input and output.

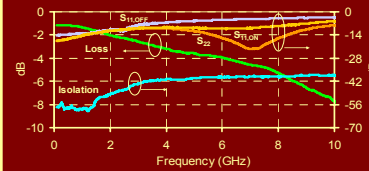
Timing Control and Impulse Generation Circuitry



- It creates the delayed version of the input pulse sequence for all 4 channels by using a path-sharing time delay architecture;
- Path-sharing architecture reduces gate count, and therefore, reduces chip area.

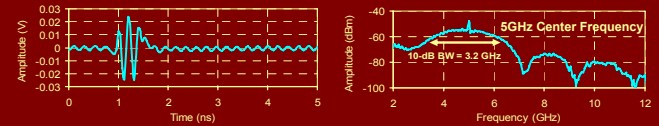
Measurement Results

Switch measured small-signal s-parameters (probed)

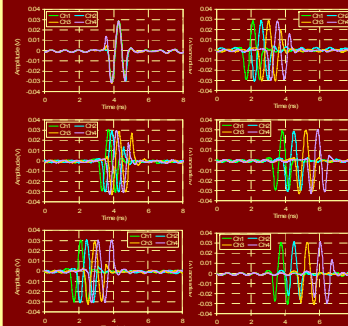


Performance (0-6GHz)	Result
Insertion Loss	< 4dB
Isolation	> 40dB

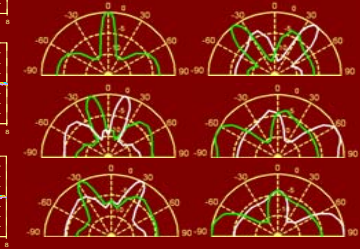
A measured pulse sinusoid with minimum pulse width



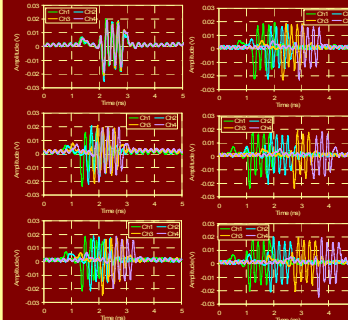
Measured 4-channel outputs at 1.3GHz



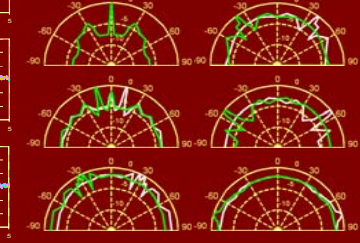
Synthesized array patterns for 22.8-cm antenna spacing, assuming *energy detector* at the receiver (in dB scale)



Measured 4-channel outputs at 5GHz



Synthesized array patterns for 26.4-cm antenna spacing, assuming *energy detector* at the receiver (in dB scale)



Performance	Result	Performance	Result
Delay Resolution between Adjacent Channels	180 ps	Maximum UWB 10-dB Bandwidth (5GHz)	3.2 GHz
Maximum Delay between Adjacent Channels	880 ps	Fabrication Process	0.13 μm CMOS

